Amendments To The Claims:

This listing of claims will replace all prior versions or listing of claims for this application:

Listing of Claims:

1. (Currently amended) An image sensor comprising:

a plurality of image sensor pixels; and

a noise reduction circuit, said noise reduction circuit being adapted to receive ~~receiving~~ a first and second amplified image ~~part at a first time~~ signals, and ~~outputting~~ being adapted to output a combination of said first and second amplified image ~~parts at said~~ signals at a first time, and ~~receiving said second image part along with~~ said noise reduction circuit being adapted to receive a third amplified image ~~at a second subsequent time~~ signal and ~~outputting~~ being adapted to output a combination of second and third amplified image ~~parts~~ signals at a subsequent time.

2. (Currently amended) A sensor as in claim 1 further comprising ~~an amplifier and~~ a fixed pattern noise reduction circuit, connected to receive said amplified image ~~parts~~ signals, and to remove at least one amplifier offset therefrom.

3. (Currently amended) A sensor as in claim 2 wherein said amplifier offset ~~is an~~ includes amplifier offsets from different rows of ~~said~~ a column.

4. (Currently amended) A sensor as in claim ~~1~~ 2 ~~further comprising at least one amplifier having~~ wherein said amplifier comprises an operational amplifier, a feedback capacitor connected across said operational amplifier, and a variable gain-setting capacitor at an input to said operational amplifier.

Claims 5-7 (Canceled).

8. (Original) A sensor as in claim 4, further comprising a reset transistor, coupled across said feedback capacitor, to reset a value of said feedback capacitor.

9. (Currently amended) A sensor as in claim 1, wherein said noise reduction circuit includes a first fixed pattern noise reduction circuit, having first and second capacitor elements respectively storing signal and reset amplified pixel values for said first amplified image signal, a second fixed pattern noise reduction circuit having third and fourth capacitors respectively storing signal and reset ~~for a second value~~ amplified pixel values for said second amplified image signal, and outputting ~~said first and second values at a first time, and outputting said second value along with a new third value at a second time to thereby re-use the second value at two different times~~ combined signal and reset values for said first and second amplified image signals at said first time.

10. (Original) A sensor as in claim 1, wherein said image sensor pixels are active pixels, each of which including a photoreceptor, and an in-pixel buffer transistor and an in-pixel selection transistor.

11. (Currently amended) A method of binning pixels, comprising:

first ~~obtaining~~ providing a plurality n of ~~pixels~~ amplified pixel signals at a first time;

adding said n ~~pixels~~ amplified pixel signals together to provide a first n-binned signal;

~~obtaining~~ second providing another plurality n of ~~pixels~~ amplified pixel signals at a second time, wherein said another plurality of ~~pixels~~ amplified pixel signals includes n-1 of the same ~~pixels~~ amplified pixel signals as obtained in said first ~~obtaining~~ providing; and

~~binning~~ adding said ~~second pixelsat a second time~~ another plurality n of amplified pixel signals to ~~produce~~ provide a second n-binned signal different from the first n-binned signal.

12. (Original) A method as in claim 11 wherein n=2.

13. (Original) A method as in claim 11 wherein n=3.

14. (Original) A method as in claim 11, further comprising removing pixel-to-pixel noise with a noise reduction circuit.

15. (Currently amended) A method as in claim 14, further comprising using at least two separate noise reduction circuits, a first of which reduces ~~offsets~~ noise in a first amplified pixel signal, a second of which reduces ~~offsets~~ noise in a second amplified pixel signal, and said first and second ~~pixels~~ amplified pixel signals being used to form said first n-binned signal, said second amplified pixel signal being retained for use with a third amplified pixel signal later processed by said first noise reduction circuit to form said second n-binned signal.

Claim 16 (Canceled).

17. (Currently amended) A method as in claim ~~16~~ 11, wherein said ~~adding~~ first providing comprises obtaining a chronologically first ~~sensed~~ amplified pixel ~~at a first time,~~ signal and subsequently obtaining a chronologically second ~~sensed~~ amplified pixel signal ~~at a second time~~, and said adding ~~the first and second sensed pixels~~ to provide said first n-binned signal comprises adding said chronologically first and chronologically second amplified pixel signals.

18. (Currently amended) A method as in claim 11, further comprising removing offsets from amplifiers that amplify said ~~pixels~~ amplified pixel signals, prior to adding said ~~pixels~~ pixel signals.

19. (Currently amended) A binning sensor, comprising:

a plurality of pixels arranged in an array;

a configurable adder, selectively connected to add ~~at least~~ a plurality n of adjacent row pixel values to one another and then to add another plurality of said adjacent row pixel values to one another, wherein said plurality n of adjacent row pixel values and said another plurality of adjacent row pixel values have at least one common row element; and

an offset reduction circuit, removing certain amplifier offsets from said pixel values prior to said adding.

20. (Currently amended) A sensor as in claim 19, wherein the number of pixels added equals n and said offset reduction circuit includes ~~first and second~~ n noise reduction circuit parts~~, each of a plurality of values in each noise reduction circuit part maintained for two cycles, and added to two different values~~.

Claims 21-23 (Canceled).

24. (New) A sensor as in claim 9, wherein said first fixed pattern noise reduction circuit is operable to store signal and reset values for said third image part on said first and second capacitors, said noise reduction circuit being operable to output combined signal and reset values for said second image part and said third image part, to thereby re-use said signal and reset values for said second image part at two different times.

25. (New) A method as in claim 17, wherein said second providing comprises obtaining a third sensed pixel signal, and wherein said adding to provide said second n-binned signal comprises adding said second and third sensed pixel signals.